CLAIMS

We Claim:

1. A method of testing a semiconductor memory having transparent error correction, the method comprising:

providing a test data pattern to the semiconductor memory;

generating a corresponding error correction code (ECC) value in response to the test data pattern;

storing the test data pattern and the corresponding ECC value in a memory array;

reading the test data pattern and the corresponding ECC value from the memory array;

passing the test data pattern unmodified as an output data value if no errors exist in the test data pattern and the corresponding ECC value;

correcting a single-bit error in the test data pattern and the corresponding ECC value if a single-bit error exists in the test data pattern and the corresponding ECC value, and passing the resulting test data pattern as an output data value; and

ensuring that an erroneous test data pattern having one or more error bits is provided if the test data pattern and the corresponding ECC value include a multiple-bit error, and passing the erroneous test data pattern as an output data value.

2. The method of Claim 1, wherein the step of ensuring that an erroneous test data pattern having one or more error bits is provided if the test data pattern and the corresponding ECC value include a multiple-bit error comprises:

identifying a set of test data patterns that cause all potential multiple-bit faults in the memory array to be excitable; and

selecting the test data pattern from the set of test data patterns.

3. The method of Claim 1, further comprising:

generating a set of check bits in response to the test data pattern read from the memory array; and

comparing the set of check bits with the ECC value read from the memory array.

4. The method of Claim 3, further comprising:

generating a syndrome word in response to step of comparing the set of check bits with the ECC value read from the memory array;

activating a single-bit error signal if the syndrome word indicates the presence of a single-bit error; and

activating a multiple-bit error signal if the syndrome word indicates the presence of a multiple-bit error.

5. The method of Claim 3, further comprising:

generating a syndrome word in response to step of comparing the set of check bits with the ECC value read from the memory array;

activating a single-bit error signal if the syndrome word indicates the presence of a single-bit error; and

activating a multiple-bit error signal if the syndrome word indicates the presence of an even number of errors.

6. The method of Claim 4, wherein the syndrome word indicates the location of a single-bit error in the test data pattern and the ECC value.

7. The method of Claim 1, wherein the step of ensuring that an erroneous test data pattern having one or more error bits is provided if the test data pattern and the corresponding ECC value include a multiple-bit error further comprises inverting one or more bits of the test data pattern.

8. The method of Claim 1, wherein the ECC value is generated using an odd-weight Hamming code.

9. A method of testing a semiconductor memory having transparent error correction, the method comprising:

applying a plurality of test data patterns to the semiconductor memory, wherein the semiconductor memory internally generates corresponding error correction code (ECC) values in response to the test data patterns;

storing the plurality of test data patterns and corresponding ECC values in a memory array of the semiconductor memory;

retrieving the plurality of test data patterns and corresponding ECC values from the memory array;

providing the retrieved test data patterns unmodified as output data values when no errors exist

in the retrieved test data patterns and corresponding ECC values;

correcting single-bit errors in the retrieved test data patterns if single-bit errors exist in the retrieved test data patterns, and providing the resulting test data patterns as output data values; and

ensuring that erroneous test data patterns having one or more error bits are provided if multiple-bit errors exist in the retrieved test data patterns and the corresponding ECC values, and passing the erroneous test data patterns as output data values.

10. The method of Claim 1, wherein the step of ensuring that erroneous test data patterns having one or more error bits are provided comprises, inverting one or more bits of the retrieved test data pattern.

11. The method of Claim 9, further comprising determining whether each of the retrieved test data patterns and corresponding ECC values contain multiple-bit errors.

12. The method of Claim 11, wherein the step of determining whether each of the retrieved test data patterns and corresponding ECC values contain multiple-bit errors comprises determining whether each of the retrieved test data patterns and corresponding ECC values contain an even number of bit errors.

13. The method of Claim 9, wherein each of the test data patterns has a width of N-bits, wherein N is an integer, and wherein the plurality of test patterns includes 2N or fewer test patterns.

14. The method of Claim 9, wherein the ECC values are generated using an odd-weight Hamming code.

15. The method of Claim 9, further comprising selecting the plurality of test data patterns to ensure that 100% of the multiple-bit errors in the memory array are detectable.

16. The method of Claim 9, wherein the test data patterns comprise a marching "1" pattern and a marching "0" pattern.

17. The method of Claim 9, wherein the test data patterns comprise a walking "1" pattern and a walking "0" pattern.

18. The method of Claim 9, wherein the ECC values are not accessible from outside the semiconductor memory.

19. A memory system comprising:

a semiconductor memory having a memory array, a memory interface and an error detection/correction unit, wherein the memory array is configured to store test data patterns and corresponding error correction code (ECC) values, the memory interface does not provide direct access to the ECC values, and the error detection/correction unit is configured to correct single-bit errors in the test data patterns and corresponding ECC values; and

a set of test data patterns associated with the semiconductor memory, wherein the set of test data

patterns are selected such that any multiple-bit error in a test data pattern and the corresponding ECC value causes the error detection/correction unit to provide an output data pattern having an error, thereby rendering multiple-bit faults 100% detectable.

20. A semiconductor memory device having transparent error detection and correction, comprising:

an error correction code (ECC) generator configured to provide a corresponding ECC value in response to a test data pattern;

a memory array configured to store the test data pattern and the corresponding ECC value; and

an error detection/correction circuit coupled to receive the test data pattern and the corresponding ECC value from the memory array, and in response, provide an output test data pattern, wherein the error detection/correction circuit is configured to provide the test data pattern as the output test data pattern if no errors exist in the test data pattern and the corresponding ECC value, to correct any single-bit errors in the test data pattern and the corresponding ECC value, and to ensure that one or more error bits exist in the output test data pattern if a multiple-bit error exists in the test data pattern and the corresponding ECC value.

21. The semiconductor memory device of Claim 20, wherein the error detection/correction circuit comprises:

a check bit generator configured to generate a set of ECC check bits in response to the test data pattern;

a syndrome generator/decoder configured to generate a syndrome in response to the set of ECC check bits and the corresponding ECC value, wherein the syndrome indicates the presence of no errors, the presence of a single-bit error, or the presence of a multiple-bit error in the test data pattern and the corresponding ECC value; and

an error correction unit configured to pass the test data pattern unmodified if the syndrome indicates the presence of no errors, correct a single-bit error if the syndrome indicates the presence of a single-bit error, and invert one or more bits of the test data pattern if the syndrome indicates the presence of a multiple-bit error.

22. The semiconductor memory device of Claim 21, wherein the syndrome generator/decoder is configured to indicate the presence of an even number of bit errors in the test data pattern and the corresponding ECC value.

23. The semiconductor memory of Claim 20, further comprising a plurality of test data patterns associated with the error detection/correction circuit, wherein all multiple-bit errors in the test data pattern and the corresponding ECC value are 100% controllable (excitable) and observable (detectable) via the test data patterns.